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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/046,671	03/24/1998	MASATO TAKITA	P8077-8003	2422

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EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/046,671	TAKITA ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s) _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other

DETAILED ACTION

Grounds for Rejection

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Kenichi et al.

In re claim 1, Kenichi et al. (herein referred to as Kenichi) shows in Figure 1 and related text a semiconductor device including: a lightly doped semiconductor substrate (1) of a first conduction type; a buried semiconductor layer (7) of a second conduction type formed in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate; a semiconductor region (3/5) of the second conduction type extending from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer; and a semiconductor region (6) of the first conduction type formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type, wherein a concentration of an impurity of the semiconductor region of the first conduction

type is substantially equal to a concentration of an impurity of the semiconductor substrate.

In re claim 2, Kenichi further includes a first semiconductor element formed in the first conduction type region; and a second semiconductor element formed in a second region different from the first region of the semiconductor substrate, wherein the first conduction type semiconductor region is connected to a first potential (V_{int}), and wherein the second region of the semiconductor substrate is connected to a second potential (V_{BB}) different from the first potential.

In re claim 3, Kenichi, shows wherein the second conduction type semiconductor region is extended over a third region adjacent to the first region of the semiconductor substrate; wherein the semiconductor device further includes a third semiconductor element formed in the third region of the second conduction type semiconductor region; and wherein the second conduction type semiconductor region is connected to a third potential (V_{ss}) different at least from the first potential or the second potential.

In re claim 4, Kenichi further includes a well of the first conduction type (2) formed in a fourth region in the third region; and a fourth semiconductor element formed in the first conduction type well, wherein the first conduction type well is connected to a fourth potential (V_{ext}) different from at least the first potential.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenichi in view of Applicants admitted prior art.

In re claims 5-7, Kenichi substantially discloses the invention as claimed but fails to show that the first semiconductor element and the second semiconductor element is a memory cell.

Applicants admitted prior art shows in Figure 29A a semiconductor device essentially identical to that shown in Kenichi as applied to claims 1 and 2 in that Figure 29A shows a semiconductor device including: a lightly doped semiconductor substrate (114) of a first conduction type; a buried semiconductor layer (buried portion of 138) of a second conduction type formed in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate; a semiconductor region (peripheral portions of 138 in contact with the surface of the semiconductor substrate) of the second conduction type extending from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer; and a semiconductor region (164) of the first conduction type form in the semiconductor substrate surrounded by the buried

semiconductor layer and the semiconductor region of the second conduction type, wherein the applicants admitted prior art further includes a first semiconductor element (152/154) formed in the first conduction type region; and a second semiconductor element formed in a second region different from the first region of the semiconductor substrate, and that the second region of the semiconductor substrate is connected to a first potential (V_{dd}), and wherein the second region of the semiconductor substrate is connected to a second potential different from the first potential. Applicants admitted prior art further teaches that the first semiconductor element and the second semiconductor element includes a memory cell (page 4, line 8 – page 8, line 3).

It would have been obvious to one of ordinary skill in the art to provide the first and second semiconductor element of Kenichi such that it include the teachings of the admitted prior art for an expectation of success. The motivation/suggestion would have been that the inclusion of a memory cell in equivalent first and second semiconductor elements is well known in the art and the structural selection of a type of memory cell among any semiconductor elements available on the basis of its suitability for the intended use involves only routine skill in the art.

Response to Arguments

5. Applicant's arguments filed 11/29/2001 have been fully considered but they are not persuasive.

Applicants argues, "...in Kenichi, the concentration of the impurity in the n-well 6 is not substantially equal to the concentration of the impurity in the n-type substrate 1" (page 3, line 22 – page 4, line 1). Furthermore, applicants argues, "...the concentration of the impurity in the n-well 6 must be higher than the concentration of the impurity in the n-type substrate 1..." (page 4, lines 2-3).

Nevertheless, Kenichi clearly states that "...since an impurity is not diffused except a p^{+1}-type layer 7 of the substrate 1 in the formation of a high energy implanted p^{+} type layer 7, the well 6 is the same as the formation on the substrate 1 in which no p-type impurity exist". Therefore, the concentration of the impurity in the n-well is substantially equal (see CONSTITUTION).

Furtherstill, the applicant argues that in Kenichi, "...the n-well 6 is damaged by an n-type impurity ion implantation..." (page 4, lines18-19) and that there's no motivation to combine Kenichi and the admitted prior art since "...if the memory cell of the applicants admitted prior art is formed in the n-well 6 of Kenichi, then there will be a large leak current from a capacitor..." (page 4, line 20-22, and page 5, lines 2-5).

In response to these arguments, the examiner notes that the features upon which applicant rely are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

1. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432** . The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday

through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

3. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

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